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Patel, H.N.; Hohl, J.H.; Oalusi, O.A.;

ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International, 27 Sept.-1 Oct. 1993

Pages:460 - 463

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2 Package clock distribution design optimization for high-speed and low-power VLSIs

Qing Zhu; Tam, S.;

Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on], Volume: 20, Issue: 1, Feb. 1997

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3 Embedded at-speed test probe

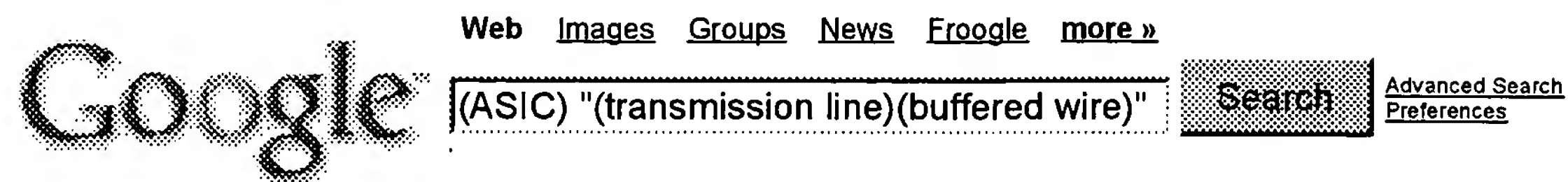
Aigner, M.;

Test Conference, 1997. Proceedings., International, 1-6 Nov. 1997

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... and implementation of an **ASIC** digital signal ... reciprocity theory; basics of **transmission line** theory and ... implementation of logic, memory, **buffer**, and conversion ...

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... The **ASIC** CHIP1 contains a bus keeper, BK1 ... that sense when the input to an output **buffer** changes ... this case we may have to consider the bus as a **transmission line**. ...

www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/Book2/CH06/CH06.2.htm - 30k - [Cached](#) - [Similar pages](#)6.10 Problems

... TABLE 6.7 Programmable **ASIC** I/O logic resources (contd ... c) What difference does it make if the output **buffer** is complementary ... 6.11 (**Transmission line** bias, 10 min ...

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... Integrated **ASIC** P&R interfaces are included; Full batch ... value selection and location, and **buffer** size selection ... **Transmission Line** and Package Modeling Solution. ...

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... **ASIC** chips can replace general-purpose commercial ... memory provides a large **buffer** that eliminates the ... resistance junctions in a **transmission line**, the impedance ...

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... In this **ASIC** event, both the CDC111/CDCVF111 ... The CDCVF111 clock **buffer** is characterized for ... the characteristic impedance (50 Ω) of the **transmission line**. ...

focus.ti.com/general/docs/lit/getliterature.tsp?baseLiteratureNumber=scaa051 - [Similar pages](#)Real World Technologies - Direct Rambus Memory, Part 1 - The ...

... provided by the memory controller **ASIC** to control ... signal both to prevent **transmission line** reflections and ... source Rambus signaling level (RSL) output **buffer**. ...

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... This can be derived from a **transmission line** by measuring the ... strength Hi, I am working on an **ASIC** that has ... I am doing hspice simulation on the output **buffer**. ...

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... means that the wire is not a wire, but a **transmission line**. ... is like a resistive load to the **buffer** with a ... determining the drive strenght needed for an **ASIC** I/O ...

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... Some **ASIC** and FPGA LVDS I/O may not be as suited ... Use a logic **buffer** to drive multiple loads and/or long ... bus may also need to be treated as a **transmission line**. ...

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... on I/O matching requirements (**ASIC**, memory, CPU ... circuits and load (such as **transmission line** balancing, cross ... contribution and input sensitivity of the **buffer**. ...

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h

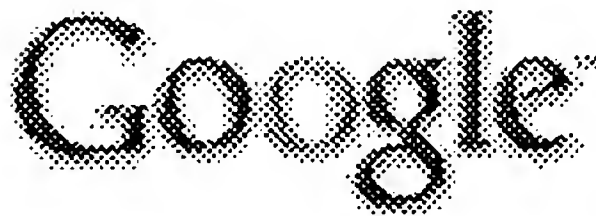
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